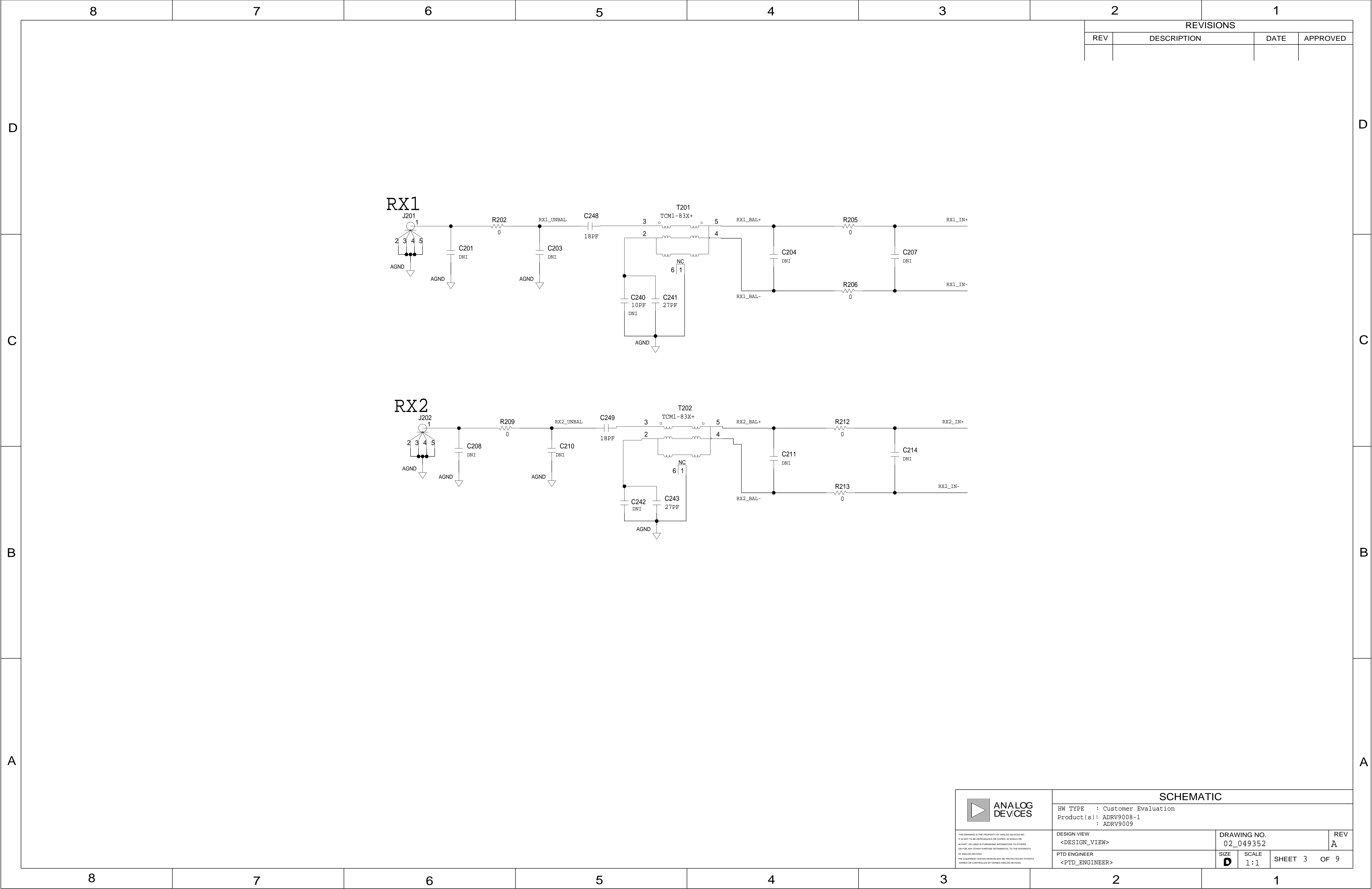


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ANALOG
DEVICES

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SCHEMATIC

HW TYPE : Customer Evaluation
Product(s): ADRV9008-1
: ADRV9009

DESIGN VIEW
<DESIGN_VIEW>

PTD ENGINEER
<PTD_ENGINEER>

DRAWING NO.
02_049352

REV
A

SIZE
D

SCALE
1:1

SHEET 3 OF 9

8

7

6

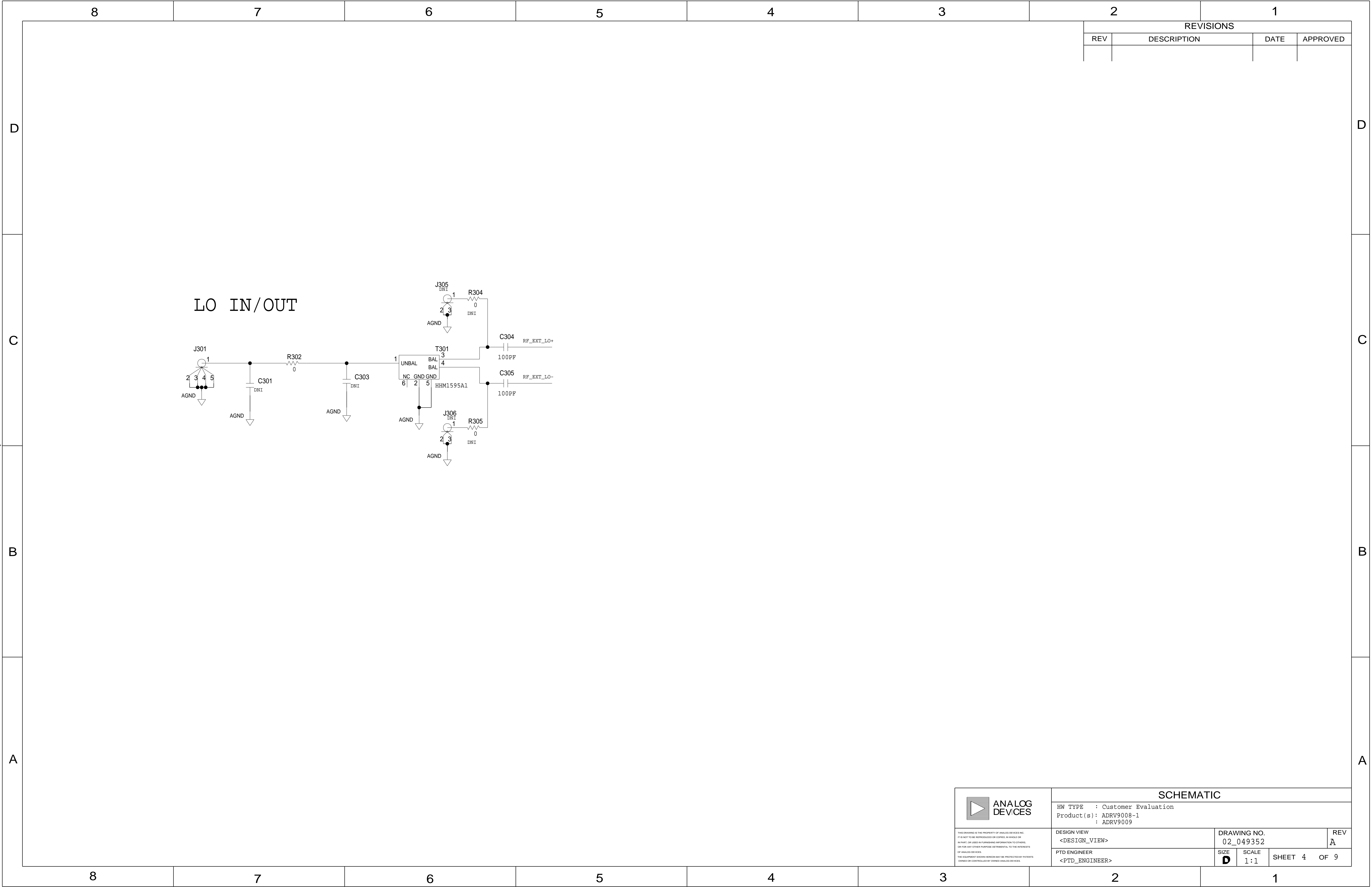
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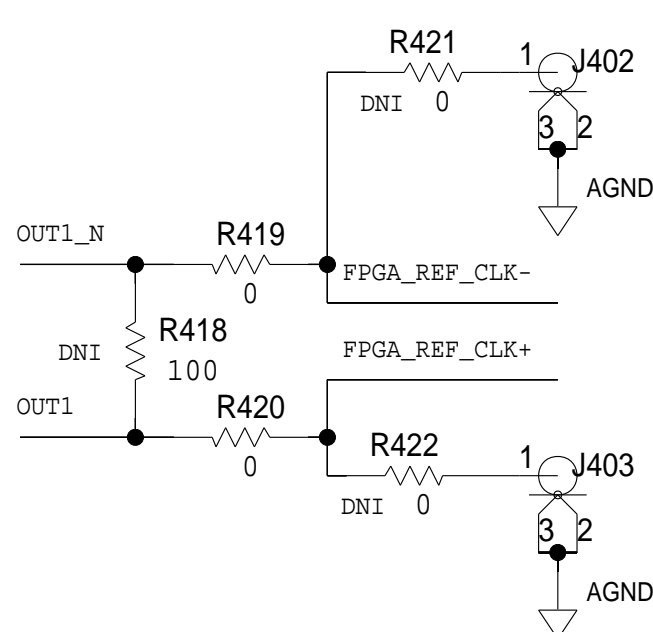
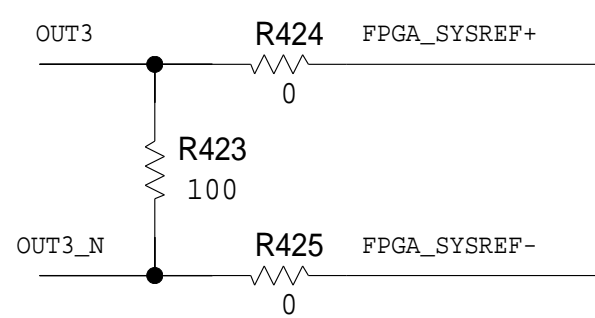
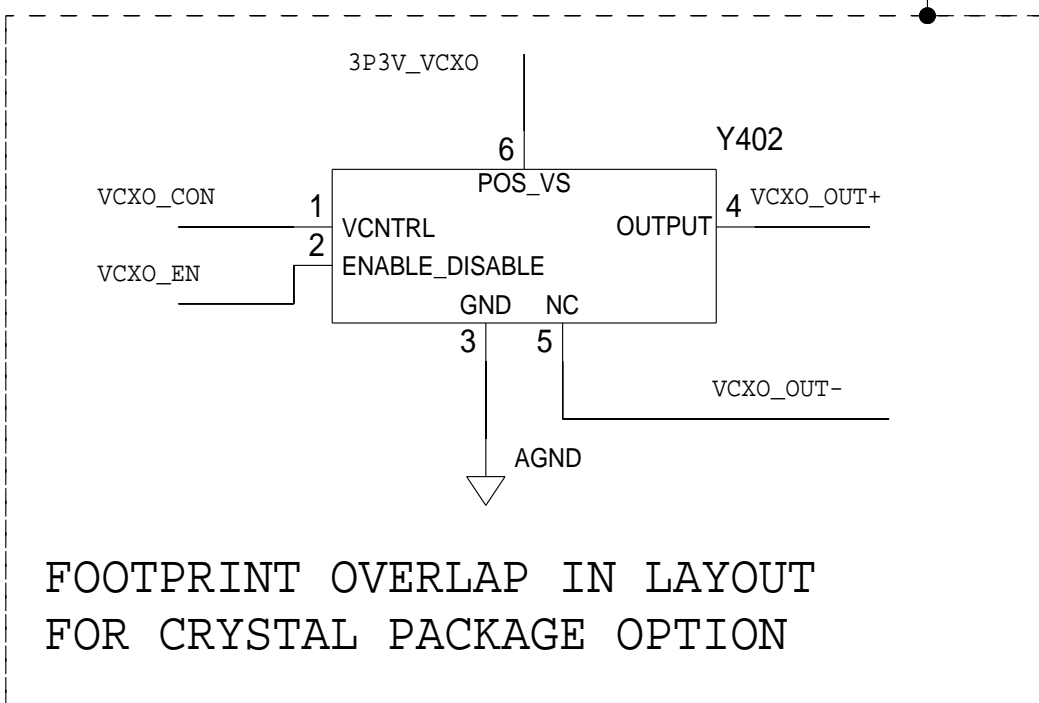
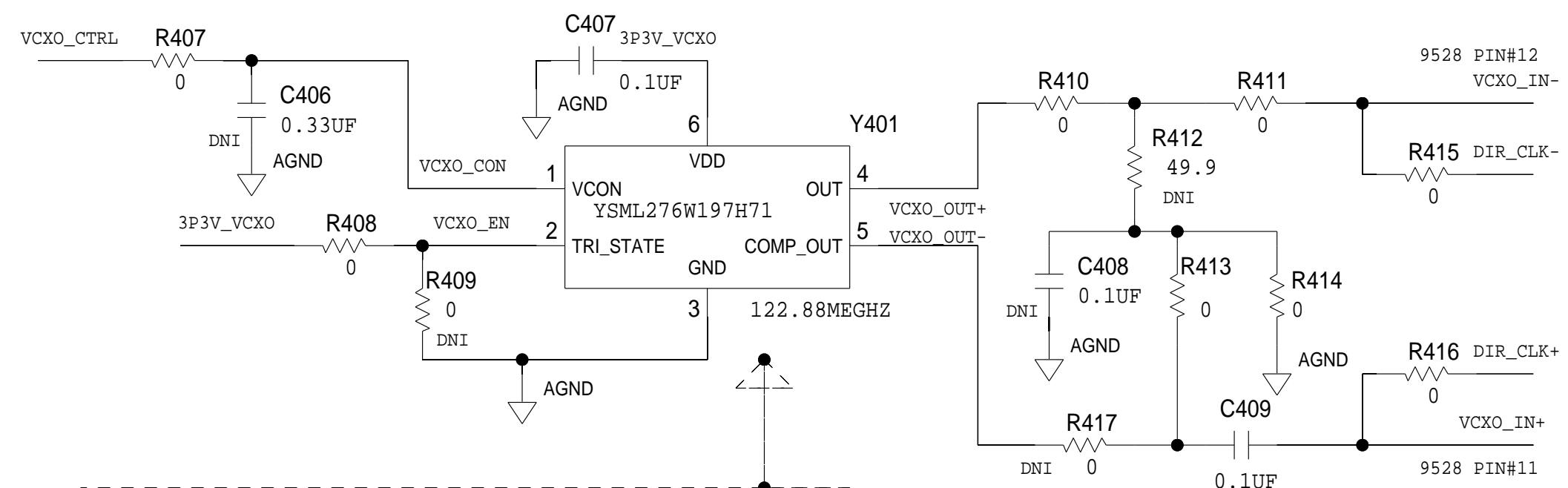
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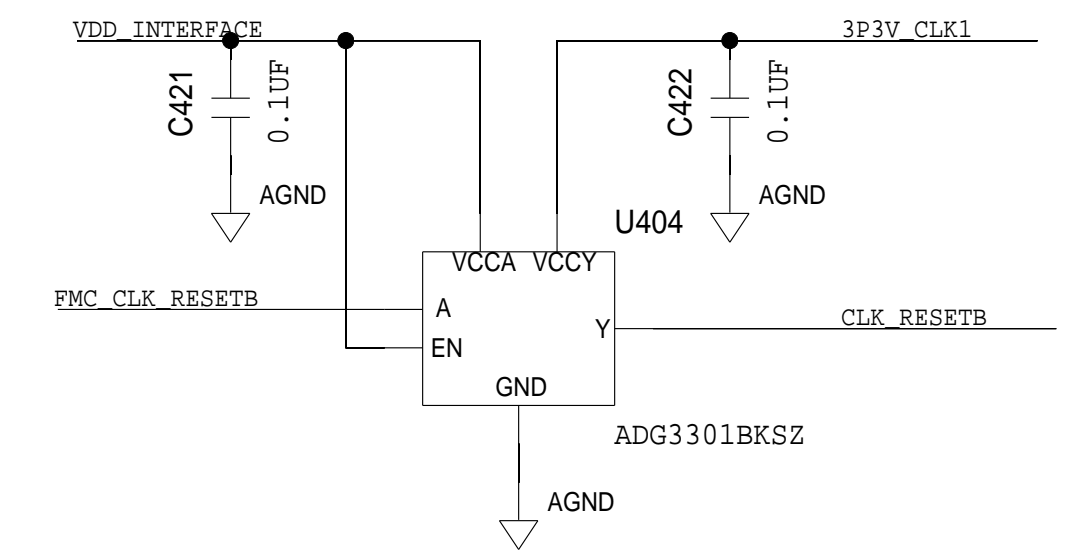
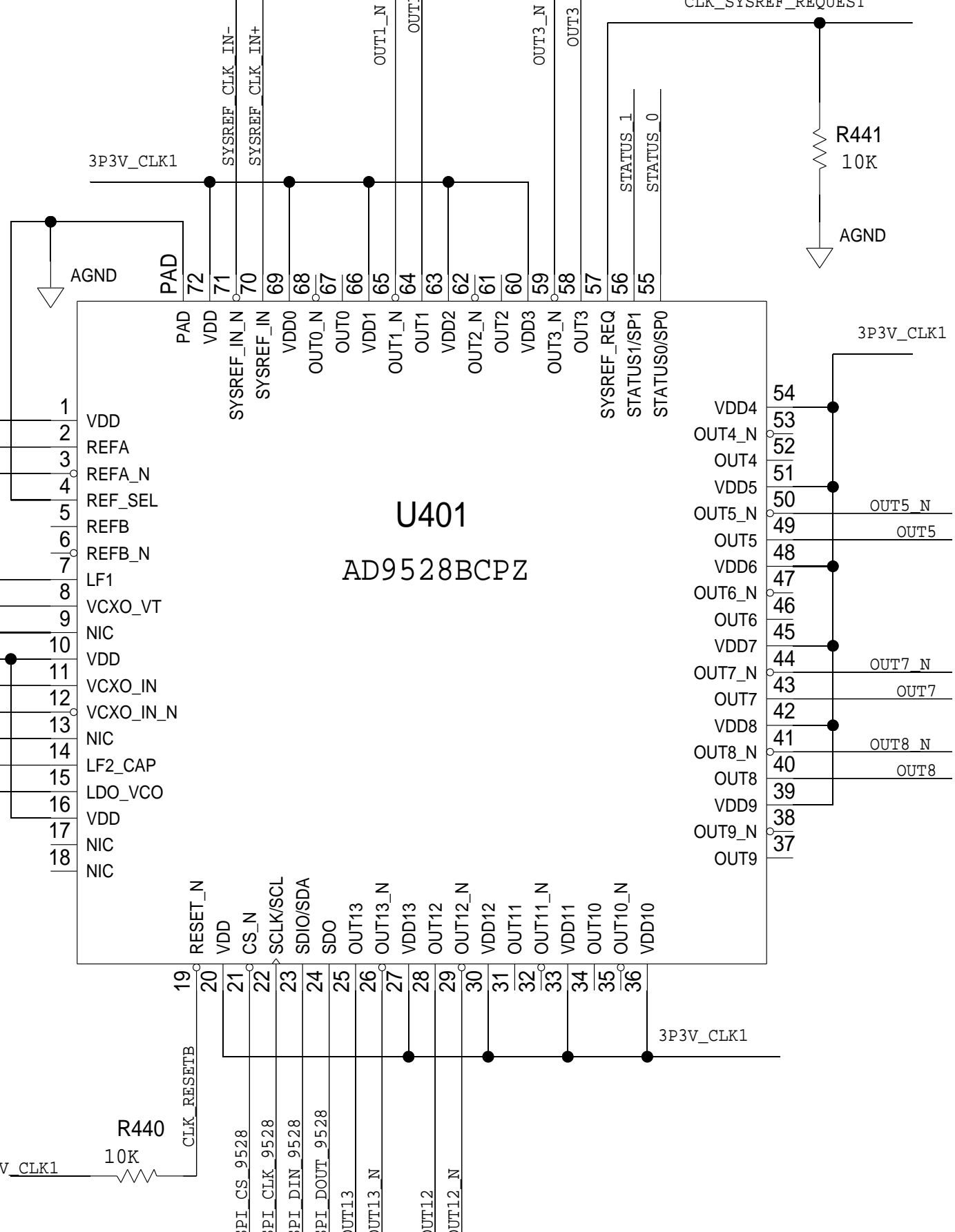
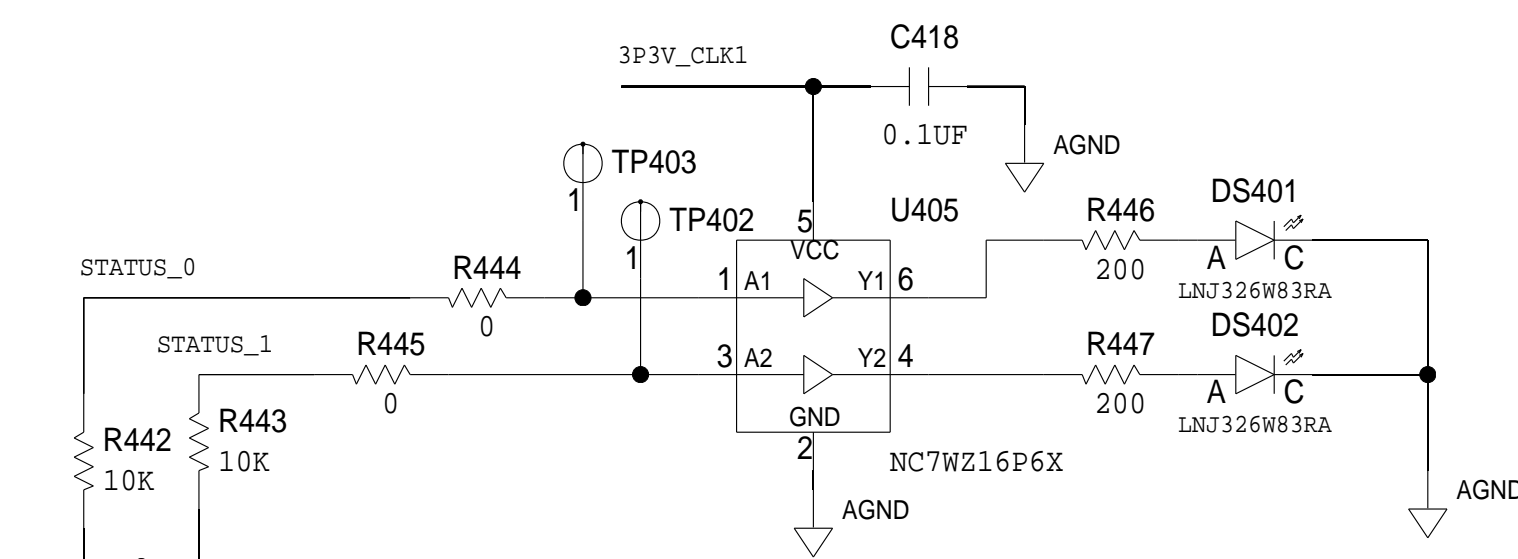
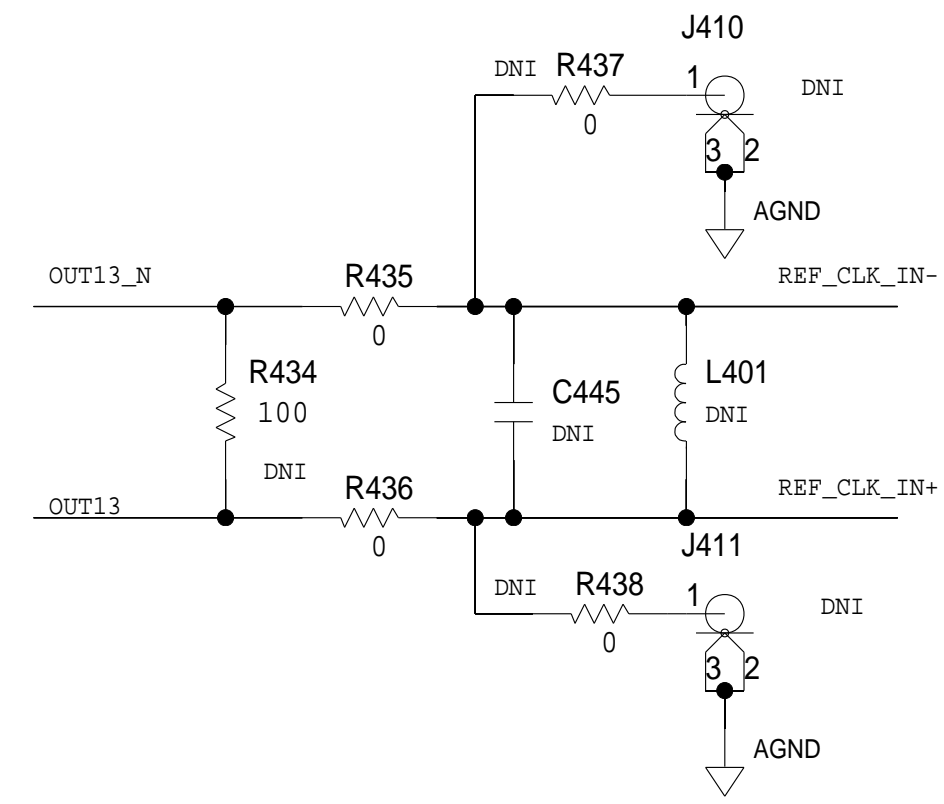
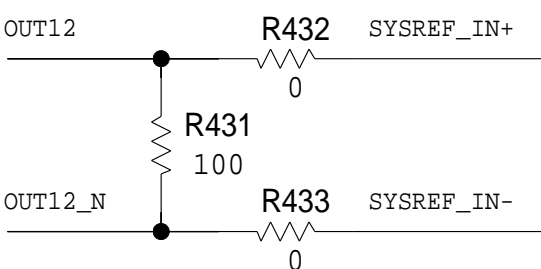
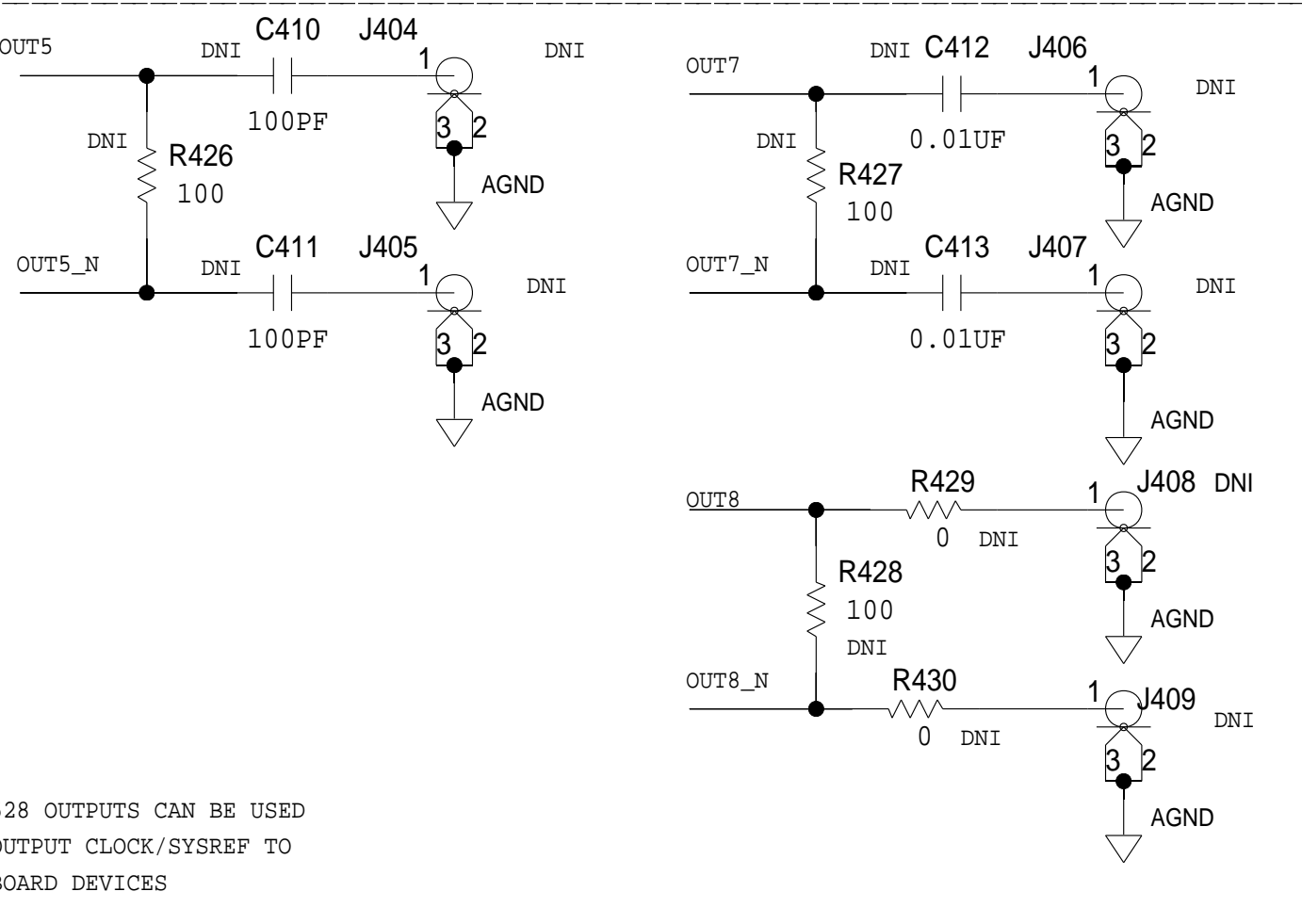
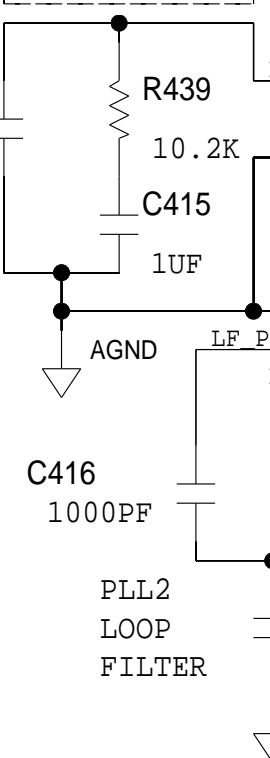
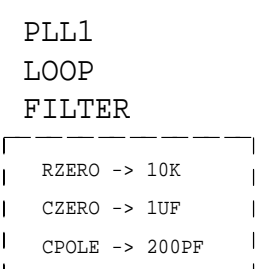
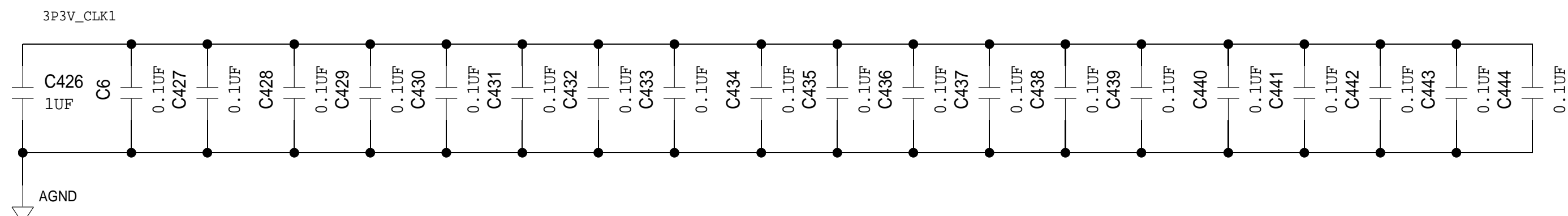
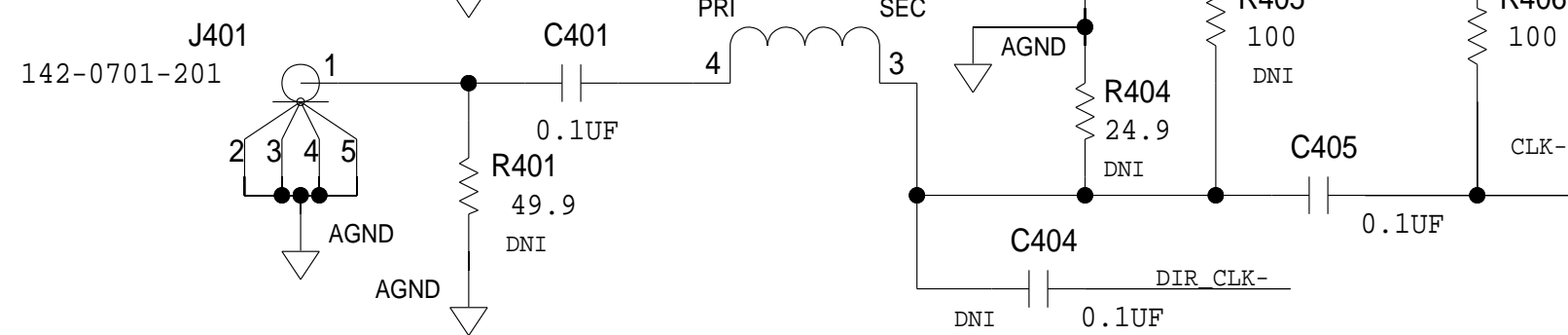
CLOCK GENERATION

REVISIONS			
REV	DESCRIPTION	DATE	APPROVED



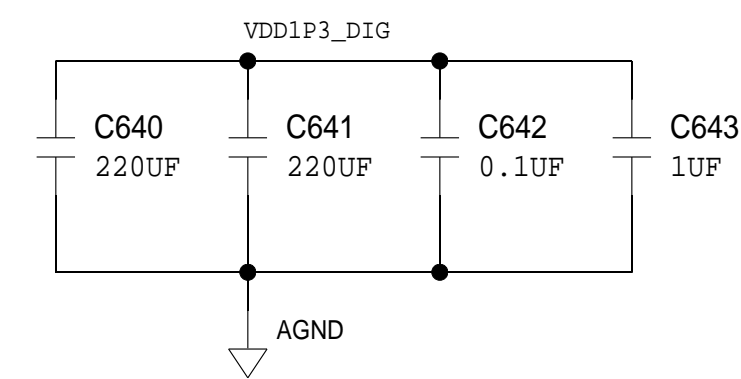
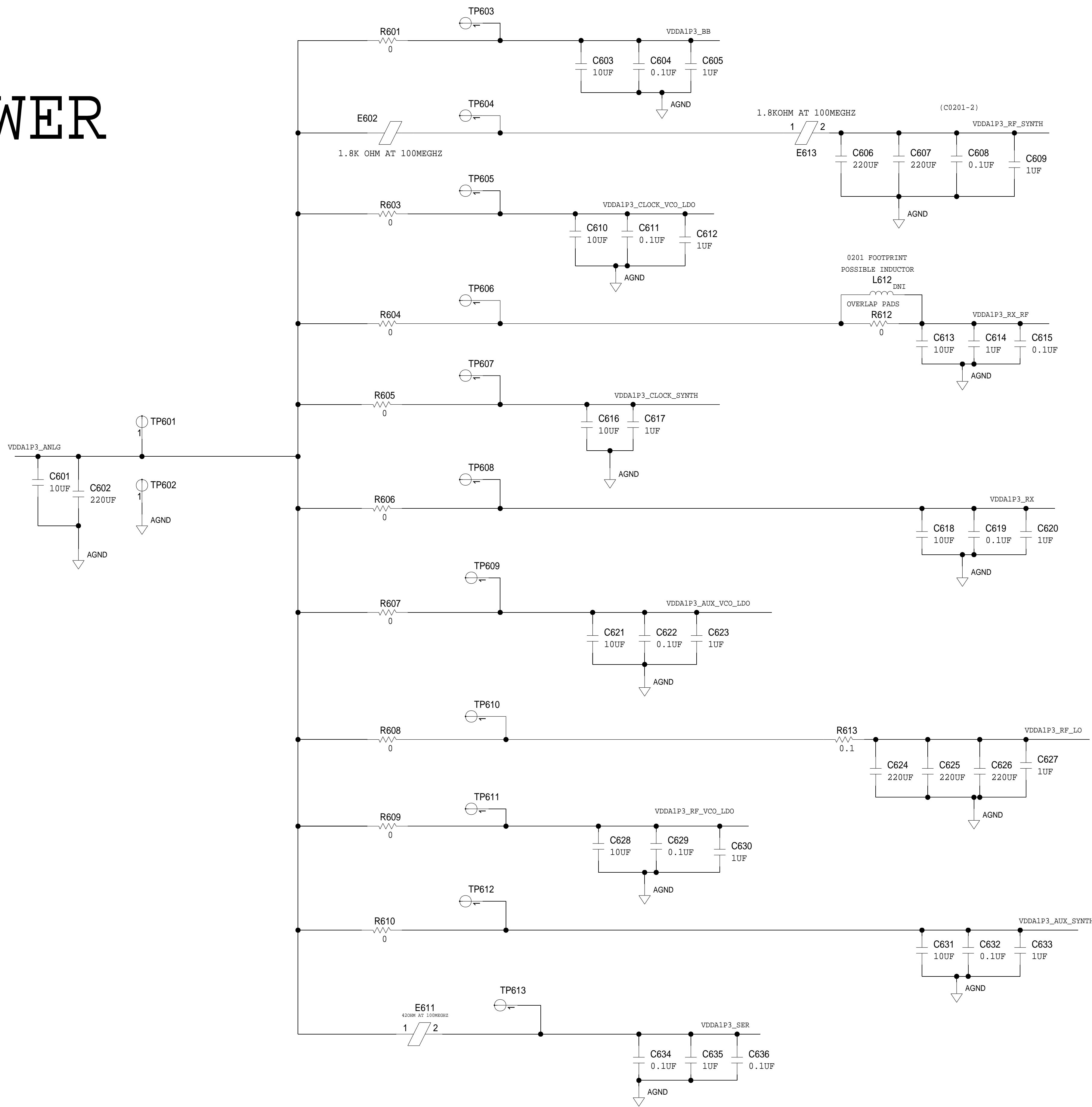
FPGA CLOCK INPUTS SELF BIASED AT 0.8V
ROUTE DIFFERENTIAL 100 OHM TRACE

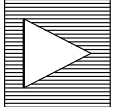
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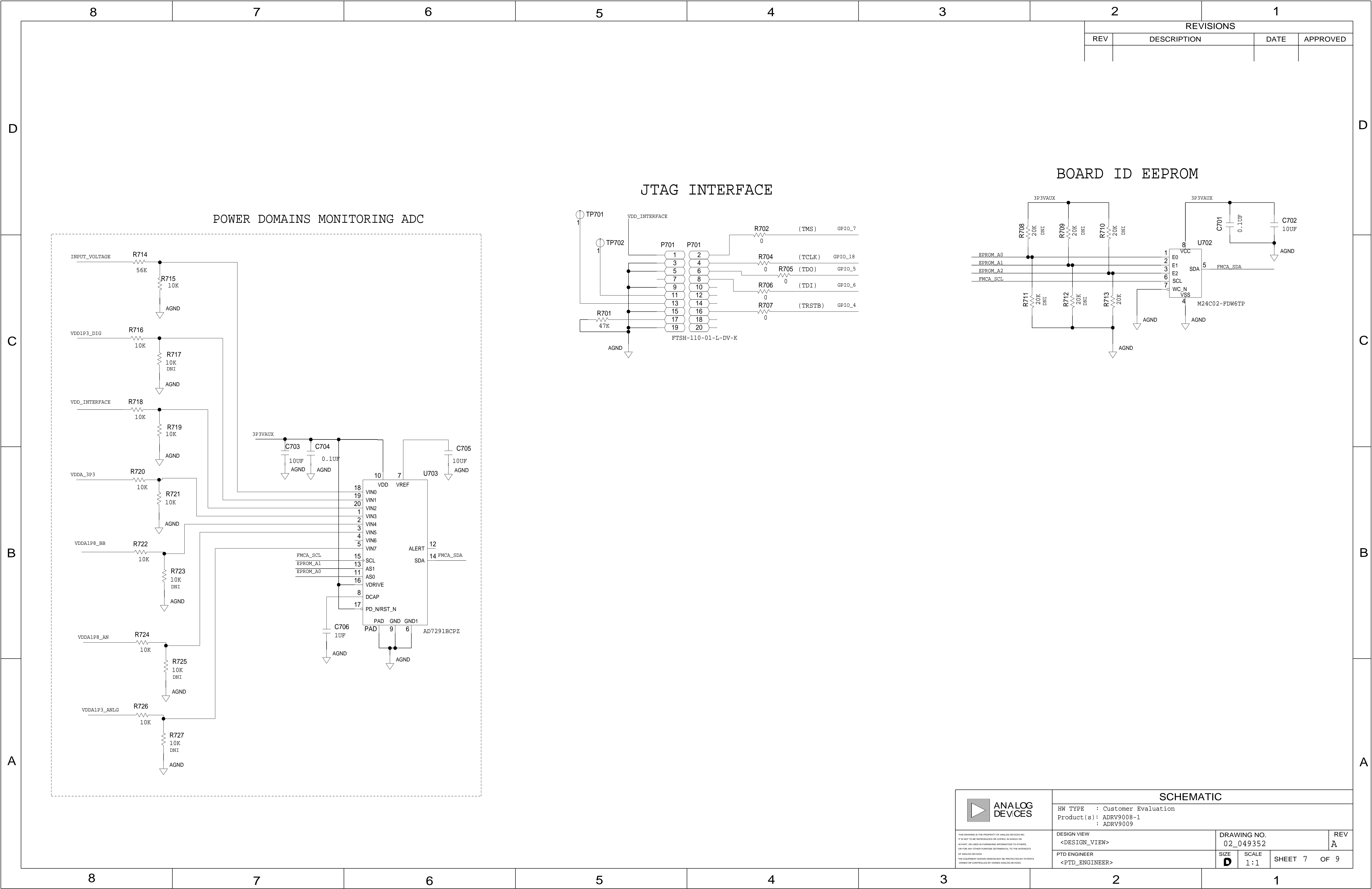


POWER

1.3VDC



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	HW TYPE : Customer Evaluation Product(s): ADRV9008-1 : ADRV9009			
	DESIGN VIEW <DESIGN_VIEW>	DRAWING NO. 02_049352		REV A
	PTD ENGINEER <PTD_ENGINEER>	SIZE D	SCALE 1:1	SHEET 6 OF 9



8

7

6

5

4

3

2

1

ANALOG DEVICES

SCHEMATIC

HW TYPE : Customer Evaluation

Product(s) : ADRV9008-1

: ADRV9009

DESIGN VIEW

<DESIGN_VIEW>

DRAWING NO.

02_049352

REV

A

PTD ENGINEER

<PTD_ENGINEER>

SIZE

D

SCALE

1:1

SHEET

7

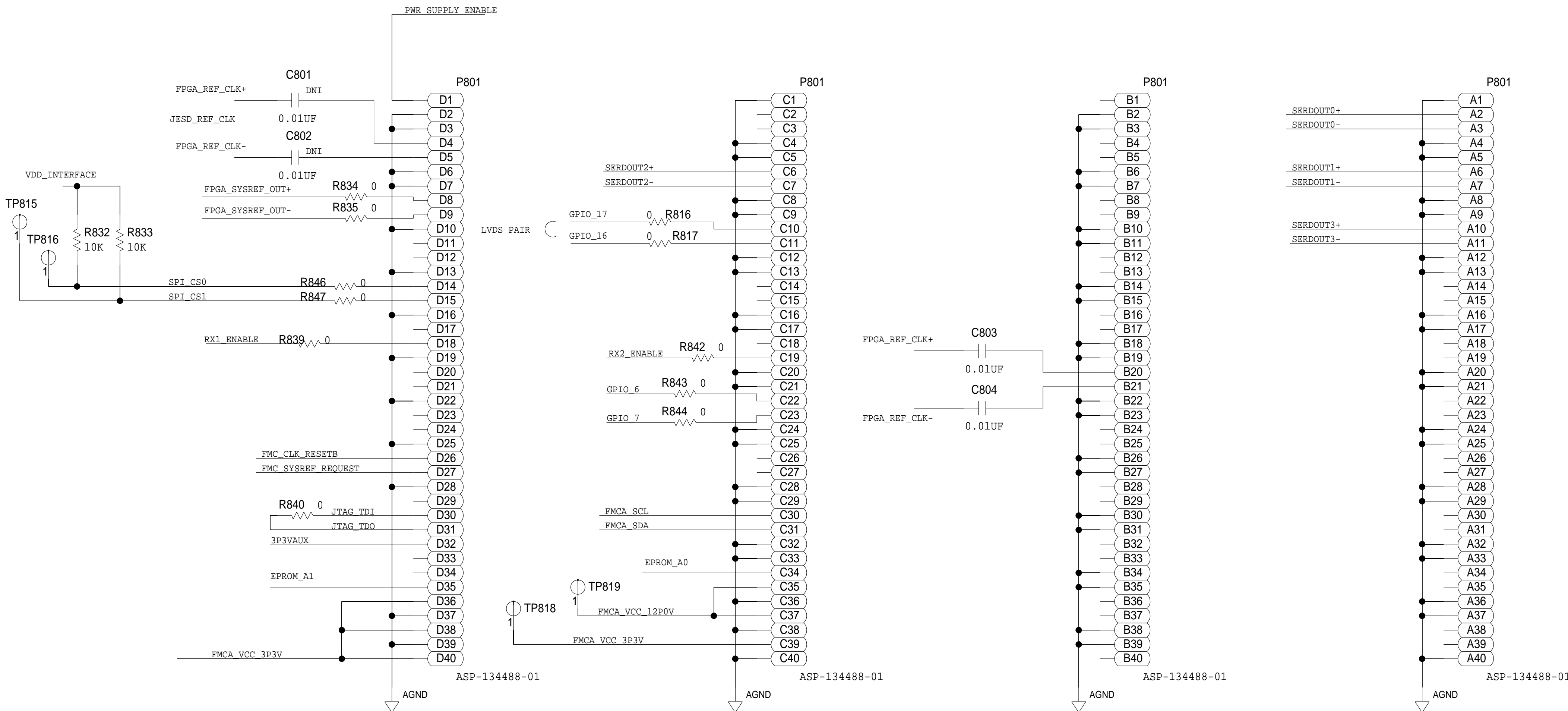
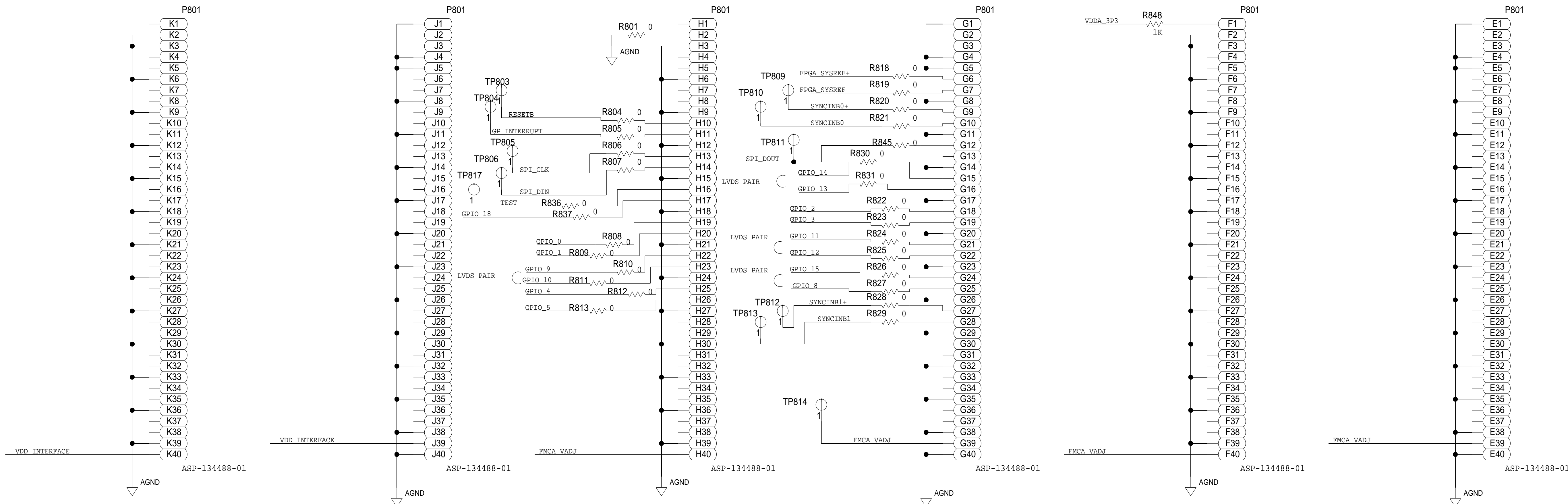
OF

9

FPGA CONNECTIONS

REVISIONS

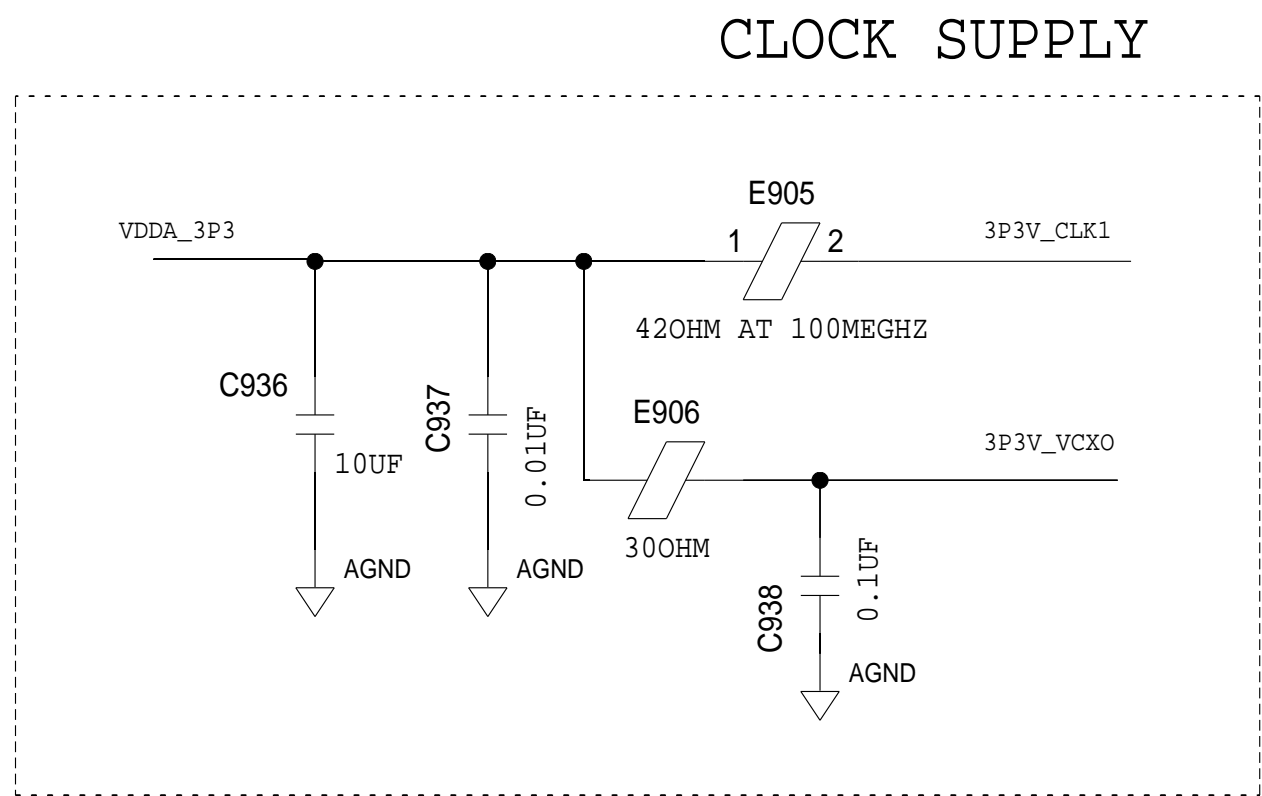
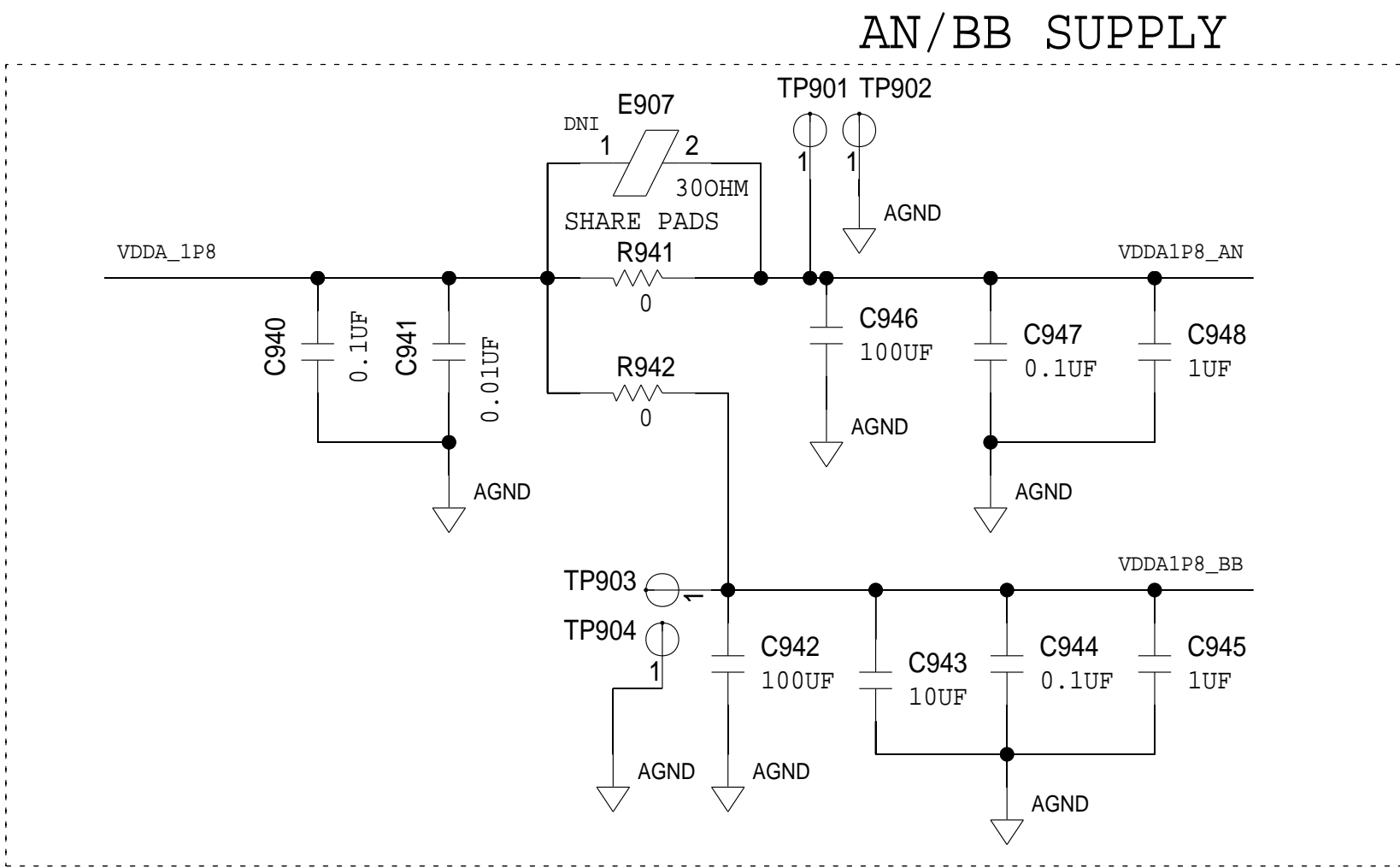
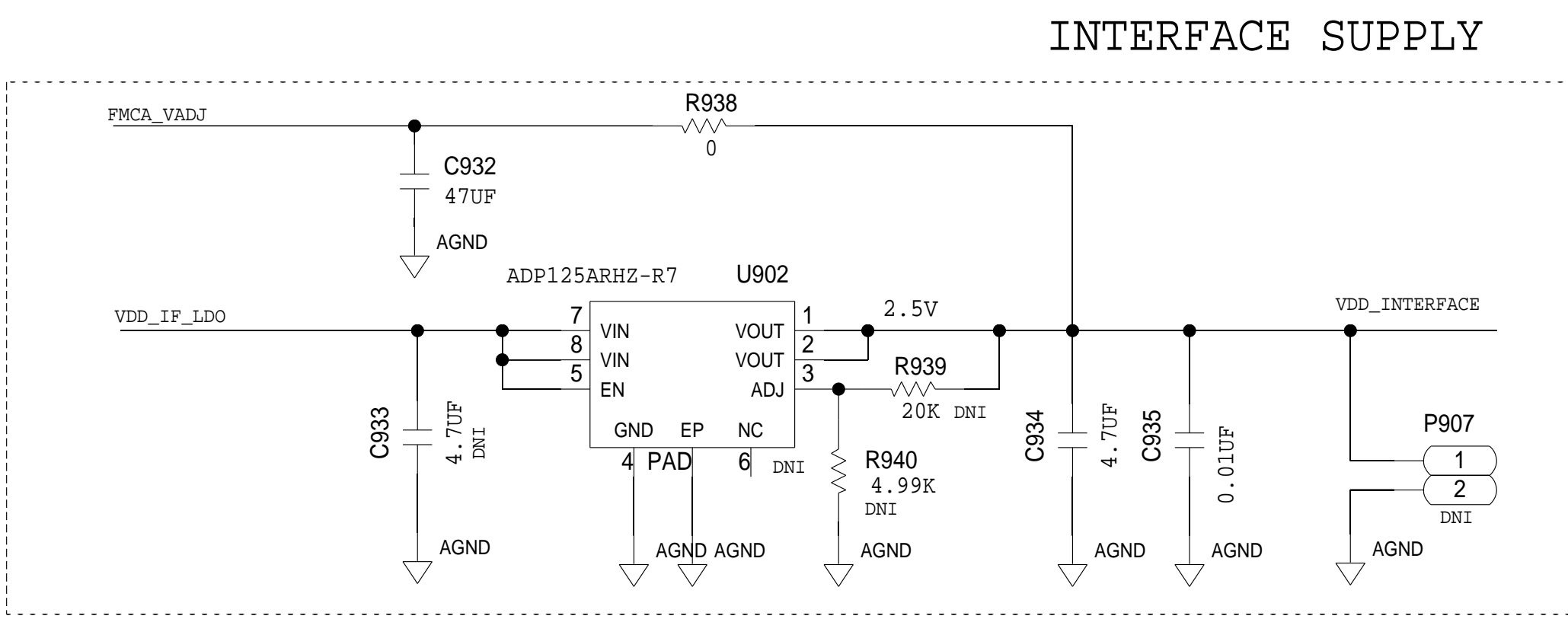
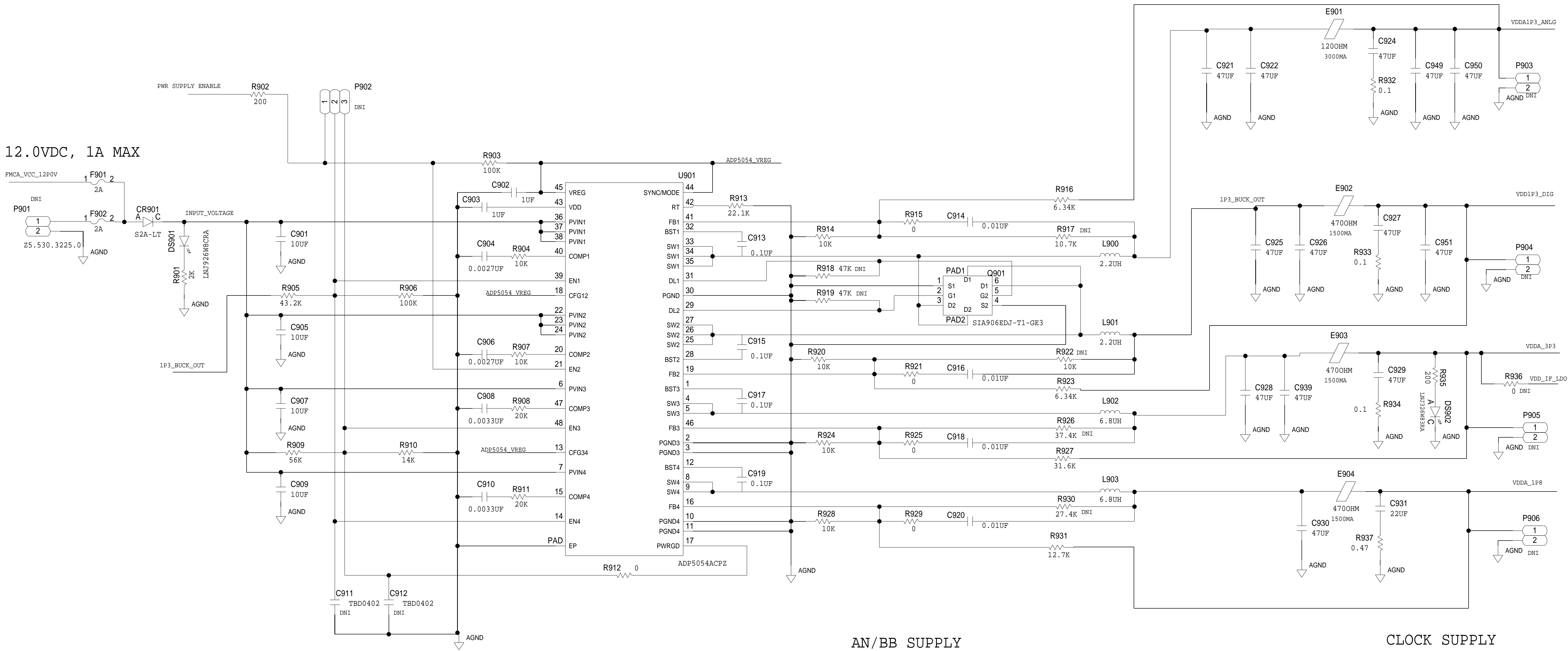
REV	DESCRIPTION	DATE	APPROVED



SCHEMATIC			
HW TYPE : Customer Evaluation Product(s) : ADRV9008-1 : ADRV9009			
DESIGN VIEW <DESIGN_VIEW>	DRAWING NO. 02_049352	REV A	
PTD ENGINEER <PTD_ENGINEER>	SIZE D	SCALE 1:1	SHEET 8 OF 9

POWER SUPPLY

REVISIONS			
REV	DESCRIPTION	DATE	APPROVED



SCHEMATIC			
HW TYPE : Customer Evaluation Product(s): ADRV9008-1 : ADRV9009			
DESIGN VIEW <DESIGN_VIEW>	DRAWING NO. 02_049352	REV A	
PTD ENGINEER <PTD_ENGINEER>	SIZE D	SCALE 1:1	SHEET 9 OF 9